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Characterisation and modelling of parasitic effects and failure mechanisms in AlGaN/GaN HEMTs

N. Malbert [a,*], N. Labat [a], A. Curutchet [a], C. Sury [a], V. Hoel [b], J.-C. de Jaeger [b], N. Defrance [b], Y. Douvry [b], C. Dua [c], M. Oualli [c], C. Bru-Chevallier [d], J.-M. Bluet [d], W. Chikhaoui [d]

[a] IMS Laboratory, Université Bordeaux 1, CNRS, ENSEIRB, 351 cours de la libération, 33405 Talence Cedex, France
[b] IEMN – Institut d'Electronique, de Microélectronique et de Nanotechnologie, CNRS – DHS – Université LILLE 1 Avenue Poincaré, BP 60069, 59652 Villeneuve d'Ascq Cedex, France
[c] ALCATEL–THALES -3-5 Lab, c/o Alcatel CIT, Route de Nozay, 91461 Marcoussis Cedex, France
[d] INL – Institut des Nanotechnologies de Lyon, CNRS, Site INSA, Bâtiment Blaise Pascal 7, Avenue Jean Capelle, 69621 Villeurbanne Cedex, France

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ABSTRACT

This work is a study of the degradations of AlGaN/GaN HEMTs induced by 2000 h of ageing tests. The methodology is based on cross-characterisation analysis.

The life tests (HTO 150 °C, HTO 175 °C and HTRB 175 °C and Idq 90 °C) have mainly induced a decrease of the saturation drain current, occurring during the first 50 h, followed by a stabilisation. There is a shift of the pinch-off voltage in the range of 0.1–0.2 V while the Schottky contact is rather stable after ageing. The evolution of the electrical characteristics after ageing does not depend on the bias conditions but rather more on the channel temperature. It seems to be neither field nor current driven. Low frequency drain current noise demonstrates that there is no trap creation and the weak evolution of the $1/f$ noise confirms that there is no degradation in the channel. Moreover, pulsed I–V measurements show a weak evolution of gate lag and drain lag rates after ageing. The same degradation mode is demonstrated for all life tests with rather high activation energy of 1.6 eV. The weak evolution of electrical characteristics observed during the life tests cannot be obviously explained by a single physical mechanism and results from a combination of trap-related effects before stabilisation.

1. Introduction

GaN based high electron mobility transistors (HEMTs) have emerged as very attractive candidates for high temperature, high-voltage, and high-power operation at microwave as well as lower frequencies [1,2]. For this reason, GaN-HEMT reliability has been addressed by an increasing number of works. The reliability implications of several aspects related to either epitaxial structure or processing have been addressed, including surface passivation [3–6], barrier thickness, Al mole fraction in the AlGaN barrier, pre-passivation plasma treatments [7], insulated gate, field-plate gate [8,9].

Physical mechanisms likely to explain degradation of electrical parameters are related to the Schottky or ohmic contacts stability and the effects of traps which are either pre-existing or generated by thermal and electrical stresses [10–12]. To gain more insight about all possible origins of degradation mechanisms, research efforts continue to focus on the implementation of various stress conditions (on and off-state DC and RF ones) while the interpretation of results include the electric-field induced strain enhancement and its related relaxation as a possible assumption [13].

The motivation for this work is the in depth understanding of the physical mechanisms that affect the carrier transport properties in AlGaN/GaN HEMTs and then penalise their performances and their reliability. As these devices suffer from the effect of traps and surface states partially coupled with material spontaneous polarization and piezoelectric effects, the methodology is based on cross-characterisation analysis.

2. Technology description

The HEMT under test were fabricated by MOCVD on SiC substrate. The epitaxial structure is composed of a buffer layer, an undoped 1.7 μm GaN layer, and an undoped 22 nm $Al_{0.24}Ga_{0.76}N$ barrier layer. The sheet resistance $R_{\square}$ is $527 \pm 33\Omega/\square$ and the bi-dimensional sheet carrier density N_S is about 1.05×10^{13} cm^{-2}.

The ohmic contacts are Ti/Al/Ni/Au evaporated stacks annealed at 900 °C for 30 s under nitrogen atmosphere. Mushroom-shaped Mo/Au 0.25 μm gates were fabricated using electron-beam lithography. The HEMT have a 2×75 μm-finger gate topology. The drain-source distance is 3.2 μm. The devices have been passivated with SiO_2/SiN (50/100 nm) using plasma enhanced chemical vapor

* Corresponding author.
E-mail address: nathalie.malbert@ims-bordeaux.fr (N. Malbert).

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deposition (PECVD). After passivation opening, the thick interconnection Ti/Pt/Au metallization is evaporated.

Specific test structures such as Transmission Line Method (TLM), Gated Transmission Line Method (GTLM) and FATFET with gate length of 100 μm are provided to allow complementary characterisation.

3. Experiments

3.1. Electrical analysis before ageing

The key-feature of the test program is to perform the analysis of device performance dispersion. Twenty-four transistors were packaged and measured under DC conditions to test both the yield and the homogeneity of the wafer. Among the tested transistors only two samples presented too high leakage current. Regarding the other devices, a good homogeneity of the main parameters is observed as shown in Table 1.

Trapping effects were studied by DC pulsed measurement using 100 ns pulse lengths with 0.3% duty cycle. Pulsed $I_{DS}(V_{DS})$ characteristics were determined for different quiescent bias points chosen to simultaneously eliminate the thermal effect and to reveal the gate and drain lag effects. At V_{DS} = 10 V, a drop of the drain current of 7.3% and 14.7% corresponds respectively to the gate lag effect and drain lag effect. These values are similar to those currently obtained for recent technologies as reported in [14].

The traps located in the devices under test have been characterised by capacitance DLTS (Fig. 1). Five trap activation energies have been identified at 0.123 eV, 0.146 eV, 0.208 eV, 0.420 eV and 0.493 eV between 100 K and 450 K (Fig. 2 and Table 2). Some of them are already known and their location is either at the surface (0.146 eV and 0.208 eV) [15] or at the heterointerface (0.420 eV and 0.493 eV) [16].

3.2. Electrical analysis after ageing

The purpose of the life tests is to compare degradations related to electrical and temperature stresses. A set of 20 packaged devices has been submitted to DC stress for 2000 cumulated hours. Four types of stress conditions were applied to the devices, defining mainly semi-on-state and off-state operation at different channel temperatures. Six devices were submitted to the following HTRB and HTO tests defined below and two devices to the I_{DQ} ageing test. The following stress conditions were set:

- High Temperature Reverse Bias test (HTRB): T_{ch} = 175 °C V_{ds} = 70 V, V_{gs} = −5 V.
- High Temperature Operation test (HTO175): T_{ch} = 175 °C V_{ds} = 25 V, I_{ds} = 62.5 mA, T_a = 41 °C.
- High Temperature Operation test (HTO150): T_{ch} = 150 °C : V_{ds} = 25 V, I_{ds} = 62.5 mA, T_a = 22 °C.
- I_{DQ} test: T_{ch} = 90 °C, V_{DS} = 50 V and V_{GS} such as I_{DS} = 30 mA.

For the HTO tests, the dissipated power was kept constant by automatic control of V_{GS}. This test is considered as the most severe because of possible hot electrons effects [10]. Drain and gate currents and voltages were monitored during the test and read-out measurements were regularly performed in situ to study the degradation.

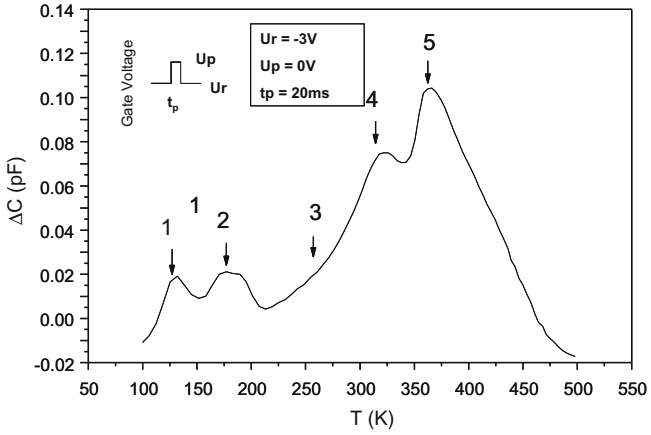

Fig. 1. Capacitance DLTS spectrum showing five contributions of traps.

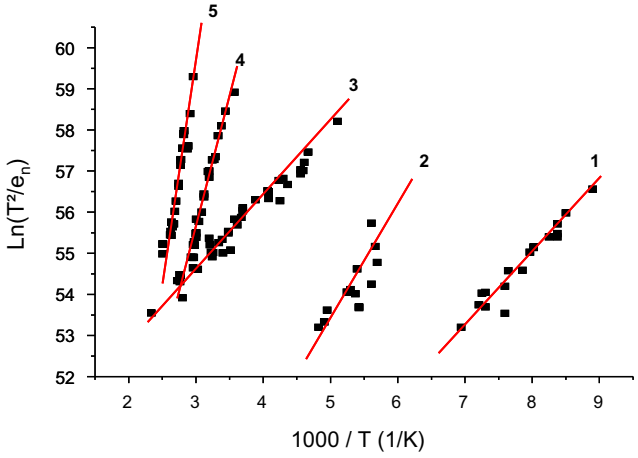

Fig. 2. Arrhenius plot for each of the five peaks recorded in the DLTS spectra.

For each stress condition, no catastrophic failure has occurred during the test and the transistors show a rather homogeneous behaviour. The gate current stays remarkably low in the range of 10 μA mm^{-1}. The variations of I_{DSS} are similar whatever the bias conditions.

Regarding the transconductance, only a slight decrease is measured between mean values of pre (313 mS mm^{-1}) and post ageing (300 mS mm^{-1}) (Fig. 3). However, the pinch-off voltage V_{th} shifts towards positive bias, weakly for the HTO test at 150 °C and HTO one at 175 °C, and more severely for the HTRB one at 175 °C. Finally, the DC characteristic of the Mo/Au Schottky diode is remarkably stable. Indeed, only few scattering of the ideality factor η, and the gate diode barrier height φ_B is observed whatever the considered life test and the reverse gate current does not present any drastic

Table 1
Average values and standard deviation of the main DC parameters.

	I_{DSMAX} mA mm^{-1} @ V_{DS} = 8 V, V_{GS} = 0	G_{mMAX} mS mm^{-1} @ V_{DS} = 8 V	I_G @ V_{GS} = −8 V (mA mm^{-1})	Gate diode ideality factor η	Gate Schottky diode barrier ϕ_B (V)
Average value	959.04	313.49	-1.46×10^{-4}	1.58	0.84
Standard deviation	18.51	33.50	–	0.51	0.16

Table 2
Signature of traps identified by DLTS (referring to Figs. 1 and 2) on virgin FATFETs.

	1	2	3	4	5
Trap density N_T (cm^{-3})	5.2×10^{16}	4.3×10^{16}	5.4×10^{16}	1.4×10^{17}	2.6×10^{18}
Activation energy E_a (eV)	0.146	0.208	0.123	0.420	0.493
Trap cross-section σ (cm^2)	8.9×10^{-19}	1.1×10^{-18}	1.8×10^{-18}	1.3×10^{-19}	2.4×10^{-14}

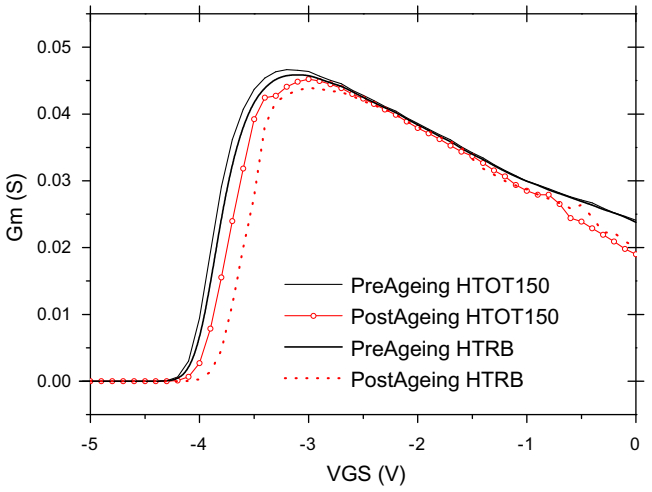

Fig. 3. Transconductance evolution measured at V_{DS} = 10 V after 1000 h of HTO test at 150 °C and HTRB one at 175 °C.

increase and is evaluated at about 1.3×10^{-4} mA mm at $V_{GS} = -8$ V.

The Table 3 summarizes the evolutions of the main electrical parameters after 2000 h of ageing tests. Almost all test conditions produced evolutions similar to those observed in HTO test. They are:

- A decrease of the saturation drain current between 7% and 13%. This reduction is all the more pronounced that the device operates close to the ohmic regime. This fact reveals an increase of the global drain-source resistance R_{on}.
- A very low evolution of the maximum transconductance while the one determined at V_{GS} of 0 V has largely decreased.
- A shift of the pinch off voltage which is comprised between 0.1 V and 0.2 V.

Moreover, when fitting the relative variation of I_{DSS} with time by a logarithmic law, the calculated slopes have similar values, demonstrating the same degradation mode:

$$\frac{\Delta I_{dss}}{I_{dss0}} = A \cdot Ln(t) + B \quad (1)$$

with $A = 6.4 \times 10^{-3}(\pm 0.1 \times 10^{-3})$ for all stress conditions. The maximum decrease of I_{DSS} is in the range of 12% after 2000 h (Fig. 4).

About 50% of the degradation takes place within the first hours of the test i.e. before 10 h.

The channel temperature is demonstrated to be the preeminent acceleration factor of the cumulative degradation of I_{DSS}. With a failure criterion of 10% decrease of I_{DSS}, an activation energy of 1.6 eV has been determined from an Arrhenius plot. Moreover, a non negligible recovery of I_{DSS}, up to 30% of the decrease has been observed during the temporary life test stopping for read-out measurements. A clear link between the stress conditions and this behaviour has not been found but this result indicates that part of the degradation is trap-related.

Pulsed $I(V)$ characteristics were measured after 1000 h and 2000 h of ageing tests. The Fig. 5 shows the overall results related to all life tests, where lag effects are observed. The mean value of the gate and drain lag rates calculated over four devices per set after 2000 h of ageing tests are reported in Fig. 6. First of all, it can be noted that on the $I_{DS}(V_{DS})$ reference characteristics obtained at V_{DS0} = 0 V and V_{GS0} = 0 V, a drop of the maximum current in the range of 10% is observed whatever the stress conditions. Furthermore, it is observed no significant change of the gate lag and drain lag rates after the HTO 150 °C and HTO 175 °C life tests while they have increased of about 3.5% after the HTRB test. In other words, neither hot electron injection nor the overall temperature has in-

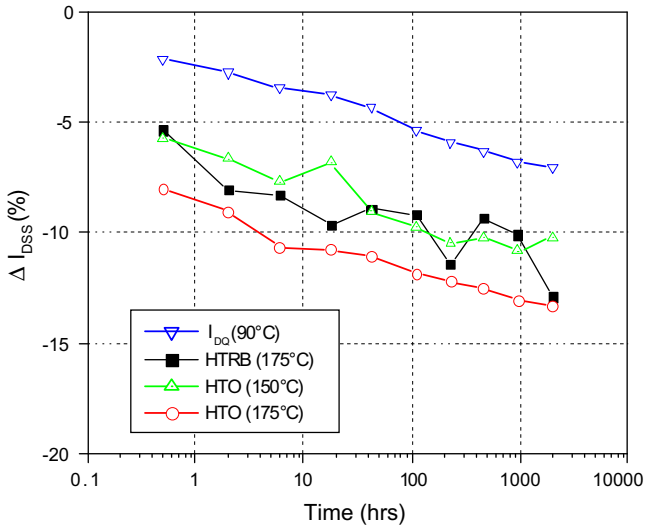

Fig. 4. Mean values of I_{DSS} degradation vs. time for the different DC life tests (logarithmic scale of time).

Table 3
Evolution of DC parameters after 2000 h of ageing tests.

Test	HTRB	HTO 175 °C		HTO 150 °C	Idq
Gate periphery (μm)	2 × 75	2 × 75	8 × 75	2 × 75	8 × 75
I_{DS} @ V_{DS} = 8 V and V_{GS} = 0 V (%)	−13	−13	−13	−10	−7
I_{DS} @ V_{DS} = 5 V and V_{GS} = 0 V (%)	−16	−17	−18	−14	−11
I_{DS} @ V_{DS} = 2 V and V_{GS} = 0 V (%)	−18	−19	−20	−17	−16
G_{mMAX} @ V_{DS} = 8 V (%)	−4.7	−4.7	−5.4	−3.7	−5
G_m @ V_{GS} = 0 V and V_{DS} = 8 V (%)	−24	−20	−25	−31	−25
Shift of V_{th} (V)	0.2	0.15	0.2	0.1	0

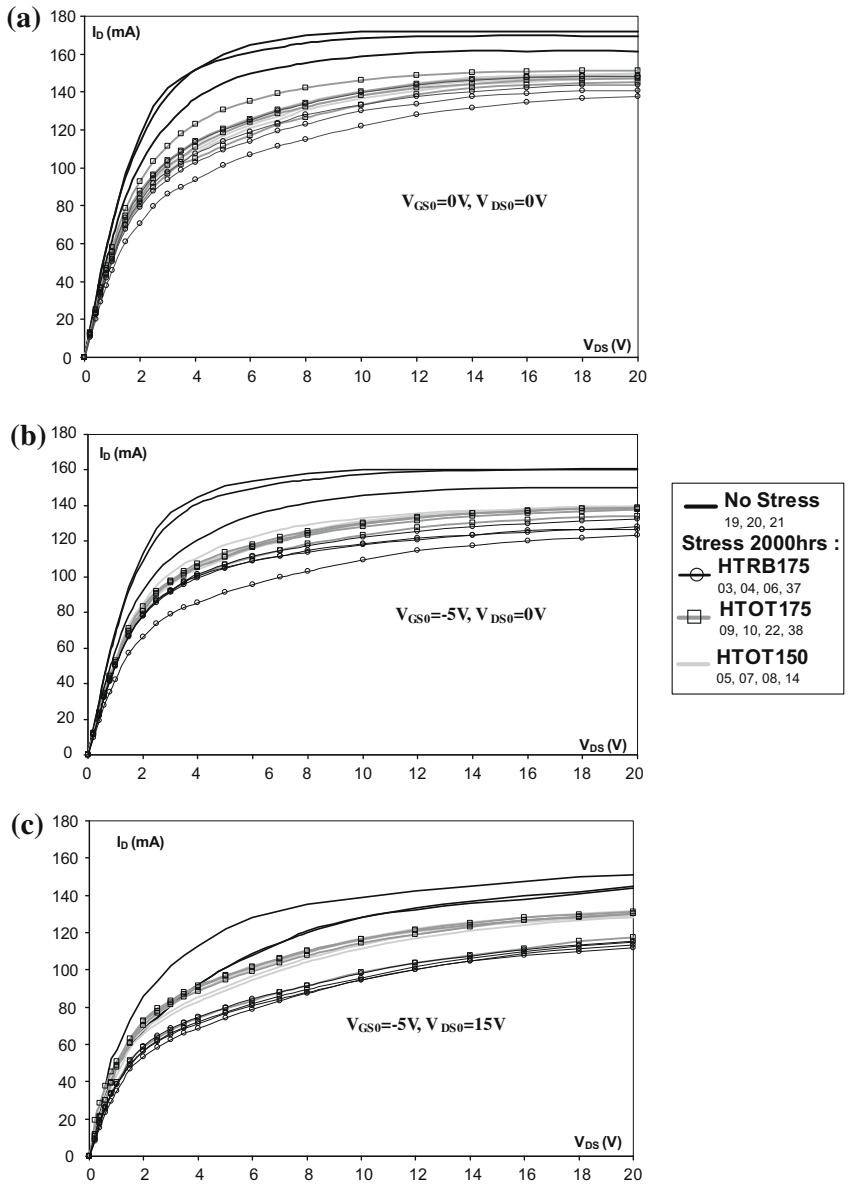

Fig. 5. DC-pulsed I_{DS}–V_{DS} characteristics at V_{GS} = 0 measured at different cold quiescent bias points on three virgin devices and on aged ones submitted to 2000 h of HTRB 175 °C, HTO 150 °C and HTO 175 °C life tests: reference characteristics (a) V_{GS0} = 0 and V_{DS0} = 0, (b) V_{GS0} = −5 V and V_{DS0} = 0, (c) V_{GS0} = −5 V and V_{DS0} = 15 V.

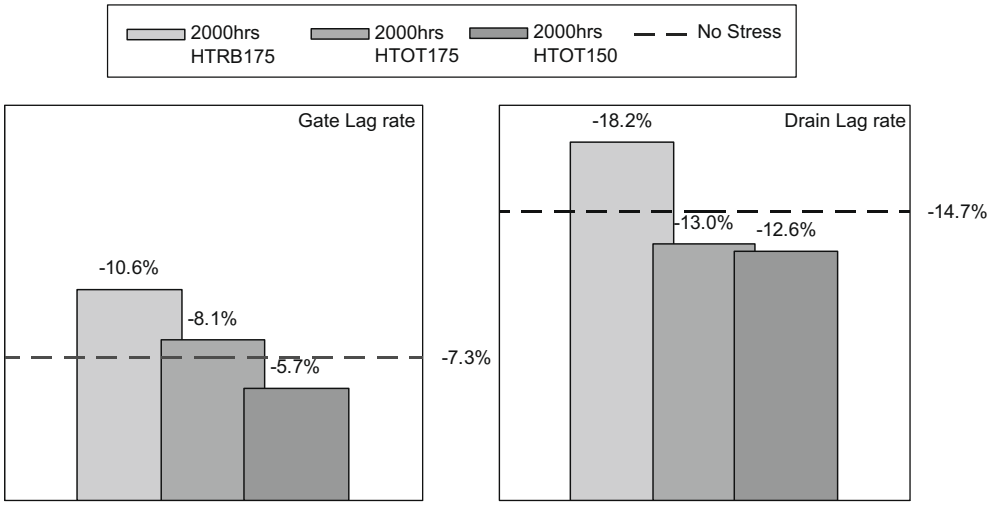

Fig. 6. Mean value of gate and drain lag rates calculated over four devices per set after 2000 h of ageing tests.

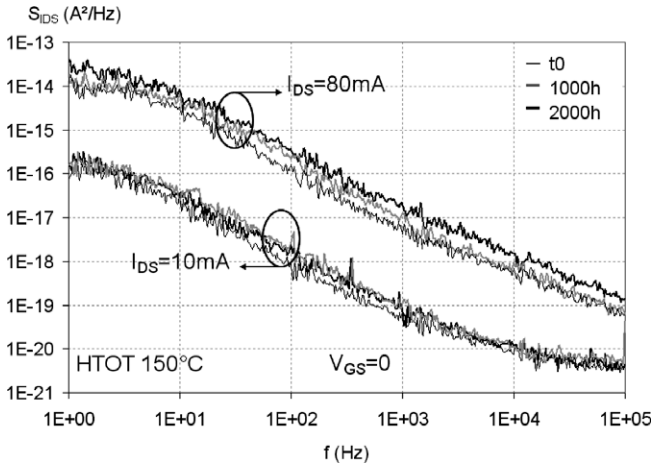

Fig. 7. Comparison of the drain current noise spectra at V_{GS} = 0 V for I_{DS} = 10 mA and 80 mA before and after the HTO 150 °C life test.

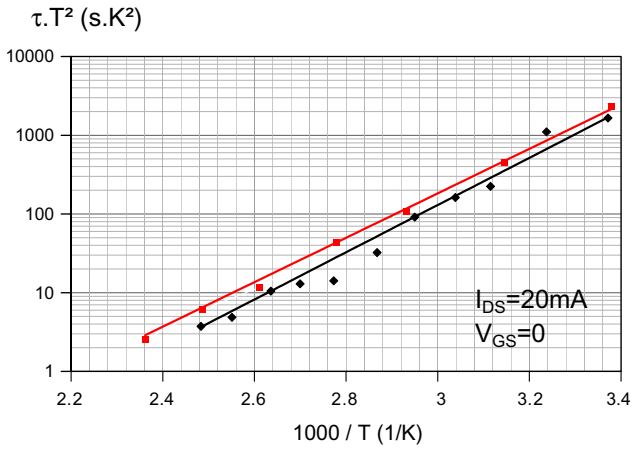

Fig. 8. Arrhenius plot showing the evolution with the temperature of the *g–r* noise cut-off frequency before (in black) and after the life tests (in red). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

duced any modification of the trap densities, as well at the barrier layer surface as in the GaN buffer.

The drain current noise spectra measured at t_0, after 1000 h and 2000 h of life test have been compared for a gate bias V_{GS} of 0 V and a drain current of 10 and 80 mA. Data plotted in Fig. 7 are related to the HTO life test performed at 150 °C. At low values of the drain current, such as I_{DS} = 10 mA, the drain current noise presents no dispersion before the life tests and a very weak increase after 1000 h and 2000 h of ageing. At higher values of the drain current such as I_{DS} = 80 mA, the LF noise has slightly increased after the HTO test at 150 °C and the HTRB life test.

For all components, the noise spectra shape has not changed after the life tests. Moreover, no new *g–r* noise component has appeared after the life tests suggesting that no new trap has been created. This result is confirmed by measurements of the drain noise spectra evolution with the temperature between 300 K and 480 K. In Fig. 8, the signature of the trap level responsible for the *g–r* noise contribution is compared before and after the life tests. An activation energy of 0.59 eV and 0.56 eV has been obtained, respectively.

The drain current noise evolution with the gate bias at a fixed drain current in ohmic regime brings information related to the noise source location responsible for the degradation. As expected, the drain current noise increases as the gate bias becomes closer to the threshold voltage of the device (Fig. 9). Indeed, the more the HEMT is biased close to the pinch off, the more predominant the noise source located in the 2-DEG channel. As the normalized 1/*f* noise level has only weakly increased after all ageing tests, it is demonstrated that the channel properties have not been affected.

4. Conclusion

The measurement of electrical characteristics shows rather low dispersion over a set of 24 virgin devices issued from the same wafer. The detailed analysis performed at 2000 h of ageing has also demonstrated reproducible behaviour over the set of 20 devices submitted to the different life tests.

Life tests (HTO 150 °C, HTO 175 °C and HTRB 175 °C and Idq 90 °C) performed during 2000 h have mainly induced a decrease of the saturation drain current, which occurs in the first 50 h followed by a stabilisation. There is a shift of the pinch-off voltage in the range of 0.1–0.2 V while the Schottky contact is stable after ageing. The evolution of the electrical characteristics after ageing does not depend on the bias conditions but rather more on the

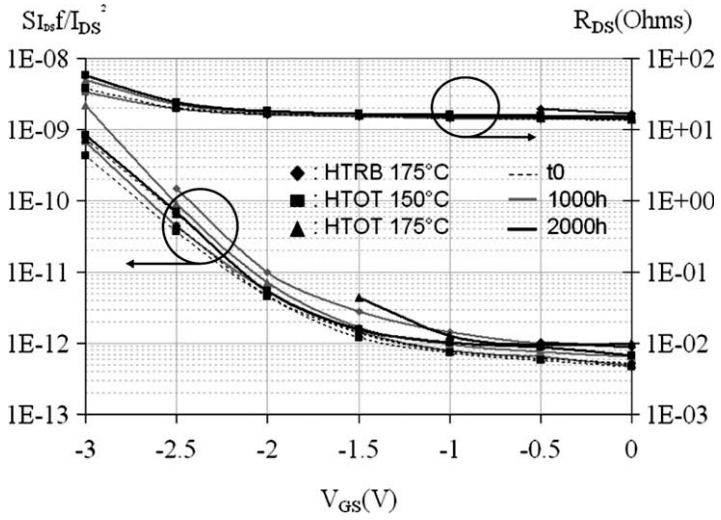

Fig. 9. Drain-source resistance and drain current noise spectral density normalized to the drain current square for devices submitted to the three life tests at t_0 and after 1000 and 2000 h of ageing test.

channel temperature. It seems to be neither field nor current driven. Low frequency drain current noise measured at 1000 h and 2000 h of life tests demonstrates that there is no creation of traps and the activation energy of the trap responsible for the *g–r* noise contribution has been determined at 0.59 ev and 0.56 eV before and after the life tests respectively. The weak evolution of the $1/f$ drain current noise confirms that there is no degradation in the channel. Moreover, pulsed *I–V* measurements show a weak evolution of the gate lag and drain lag rates.

In conclusion, the same degradation mode is demonstrated for all life tests with rather high activation energy of 1.6 eV. It could suggest the contribution of ohmic contact degradation. But, complementary ageing tests performed on TLM HEMT have demonstrated the stability of the ohmic contact resistance up to 300 °C and a drastic increase of 156% after 2000 h at 350 °C [17]. Consequently, the weak evolution of electrical characteristics observed during the life tests cannot be obviously explained by a single physical mechanism and results from a combination of trap-related effects before stabilisation.

Further RF life test confirms the DC life test results, i.e. the stability of the electrical performances after the first hours of the life test which points out the possibility of a burn-into be efficient to screen devices after the fabrication process.

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